Aiman-

Working on the memory and Stoychev requested you to send him files so he could look them over as well.

Wants Variable names the same for a similar naming convection.

“Keep going and do the rest of them” - Stoychev

Colby –

Drew out most of the schematic and has a rough outline of how it will look. Muxes and components are laid out in their specific spot. Components are in fixed locations, but wires are relative to their connection points.

Reformat code – Header file for all the const variables, methods for reducing attribute $ translate.

Wires using “Pass” so that the object is defined

Combine each component into the full project

Stoychev’s comments -

Make multiplexers wider to identify the path

The mux used for the PC update logic is flipped

Objects should be clickable – Able to see Verilog code or the internals of each component

Eric –

Fix the twos complement for the branching so it calculates negative numbers as well

Stoychev’s comments -

“This could be a freshman homework assignment”

Jacob –

Color identifier to tell what switch you are currently using

Wants to be able to use the arrows to move to each switch

Switches are scalable

Brady –

Start working on color changing of wires

Bryce –

Built most of the components of the processor

PC control needs to be built – 2 adders and a multiplexer

Single cycle process wants to be able to run by next week

Able to run at least 60 HZ