Team Name: sdmay21-38
Team Members: Colby McKinley, Aiman Priester, Eric Marcanio, Brady Kolosik, Byrce Snell, Jacob Betsworth
Report Period: March 29th - April 12th

Weekly Summary

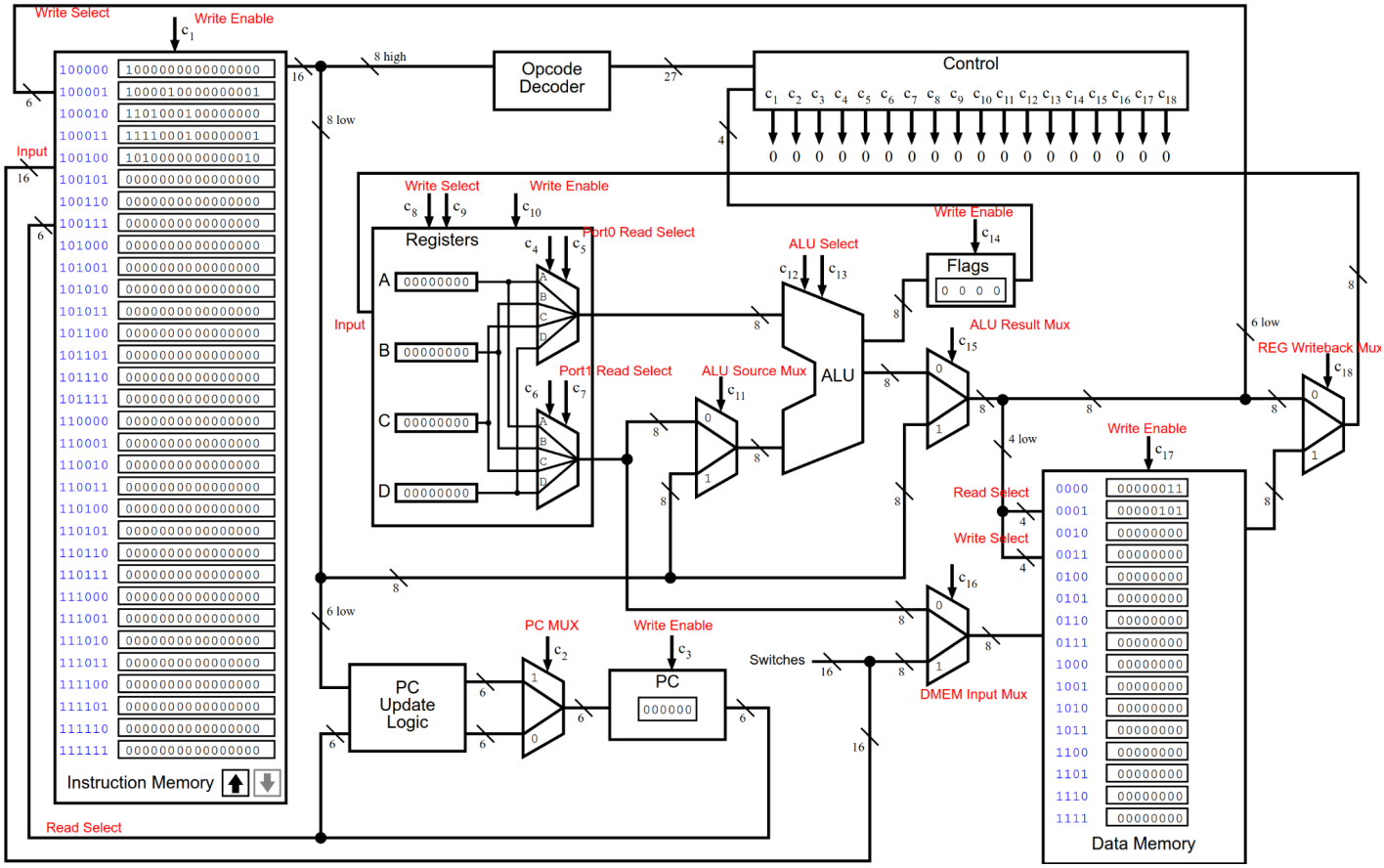
These past two weeks we have seen significant improvements in the simulator. We are able to run cycles of a program in game mode and see the propagation of a seven segment display. Also we are starting to see the visual aspects come together on the visualizer. For the most part the functionality is great but we need to work out bugs for the last few weeks of the course.

Past week accomplishments

- Eric - Assembler
    - Added a about us page to the start screen that mentions everyones name and roles
    - Added more examples that utilize the 7 segment display that could be used for testing
    - Added bootstrap to the CPU and added a nav bar
    - Made the CPU fit any screen
    - Fixed bugs that the assembler had with certain programs

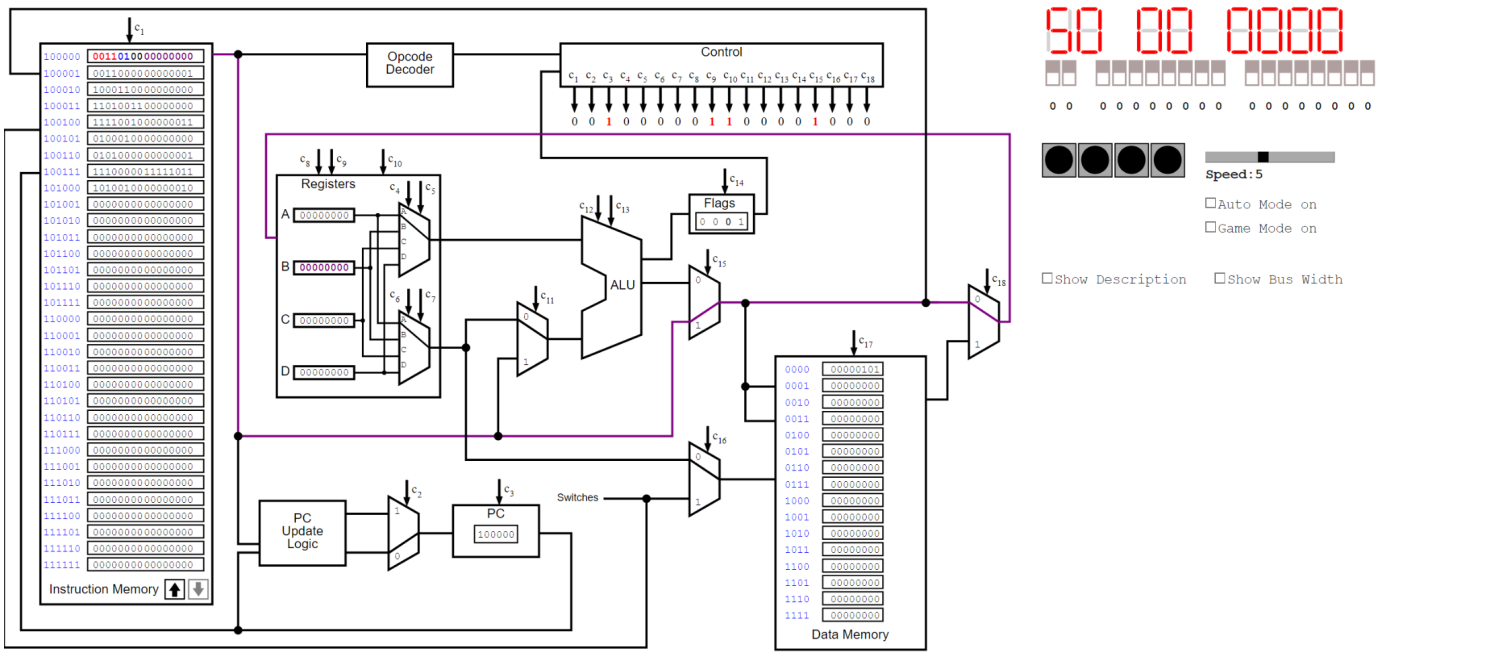
- Colby - Simulator
    - Added red description text
    - Changed arrows on IMEM and colors out gray for disabled
    - Fixed read muxes and added select function
    - Minor font changes

Senior Design Bi-Weekly Status Report; Fall 2020

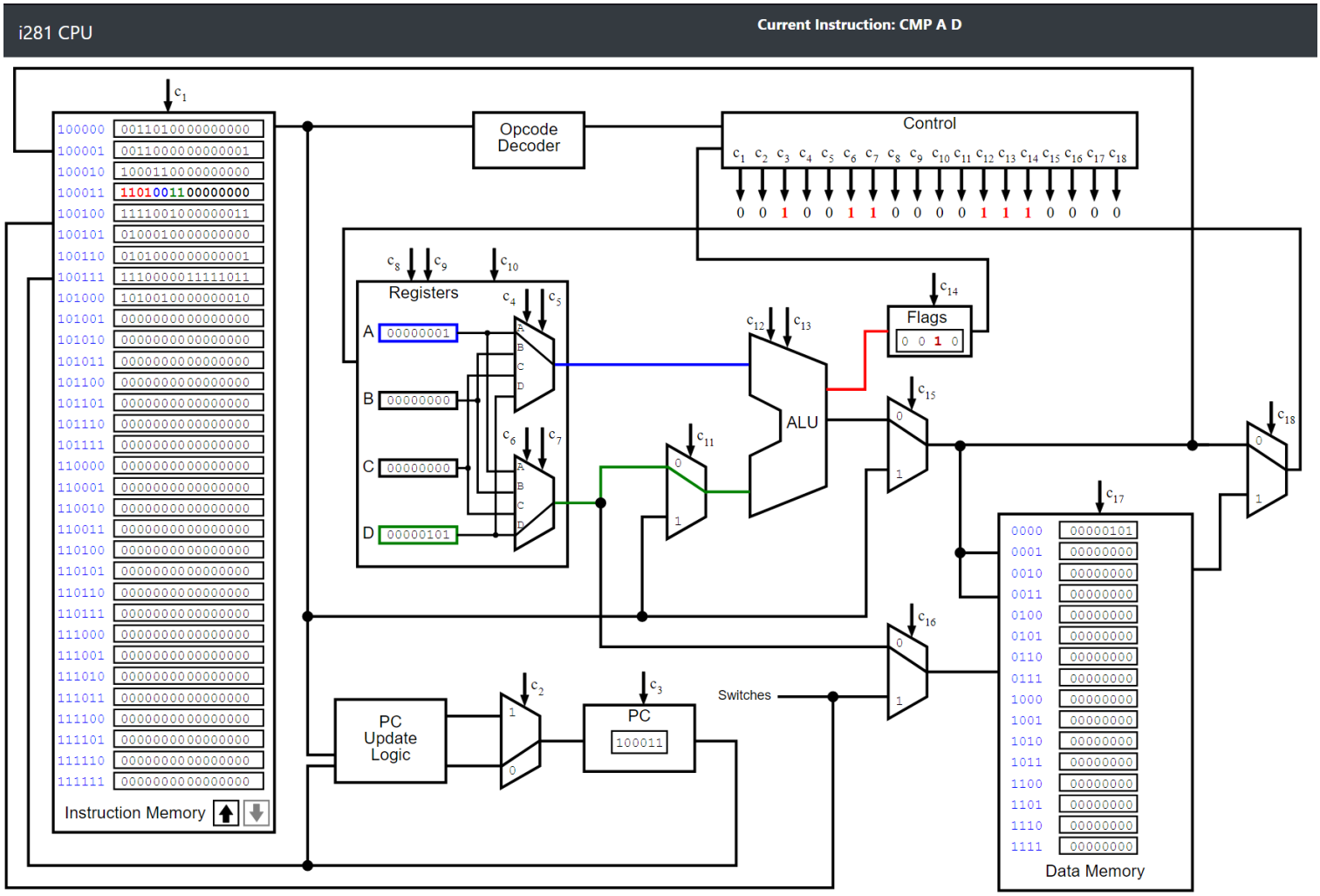


- Aiman - Verilog
  - Clients detailed pptx file has been edited and finished for the BDF files.
  - High Quality pictures have been added to the pptx file
  - Certain modifications were done to the i281 design to conform with new specifications

- Brady - Simulator
  - Syntax highlighting in the visualizer is completed
  - Proof of concept bus highlighting for instructions completed
  - Helped to solve problems with git repository
  - Debugged simulation-visualizer desync for control logic
  - Various component highlighting



Highlighting for a loadi instruction



Highlighting for cmp instruction

- Bryce - CPU Simulator
    - Fixed git issues
    - Made changes to the assembler to support larger instructions
    - Added a function to record the last pc the program executed
- Jacob - Board design
    - Added auto mode
    - Multiple visual tweaks (ex. Changed colors and sizes to look better for the layout)
    - Looking at tooltips for our svg generated text
    - Debugged seven segment issues

Pending Issues

- Eric
    - Problem with loading in certain files. They say there are errors when spacing is off. I think it is a problem due to unknown characters when switching between different IDE's
- Colby
    - No current issues
- Bryce
    - The control logic in the visualizer is a cycle behind what the simulator has
    - We need to add writeback logic to the iMem
- Jacob
    - Figure out how to make these tooltips show up
- Brady
    - Figure out control signal lagging problem
    - Writebacks happen on next cycle, how do we illustrate that?

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Eric Marcanio	New functionality on the assembler and bug fixes	**6**	**38**
Colby McKinley	GUI updates	**8**	**27**
Aiman Priester	Slide Generation / Transistor Calculations	**5**	**32**
Brady Kolosik	Completed visualizer syntax highlighting, began work on bus highlighting and program debugging.	**8**	**36.5**
Bryce Snell	Documentation and new functions	**8**	**39**
Jacob Betsworth	Visual updates and auto mode	**9**	**34**

Plans for Upcoming Reporting Period

Eric -
- Fix the bugs when uploading a document from notepad.
- Pass the name of the file being loaded in so it can be displayed in the CPU

Jacob-
- Get tooltips working
- Debug any issues that may pop up with the GUI

Bryce -
- Fix the control logic lagging
- Add iMem writeback functionality
- Check with Jacob that the switches get fixed

Colby -
- Fix positioning on some of text descriptions
- Help Brady high lighting register file

Brady-

- Continue to implement bus highlighting and component highlighting for certain instruction groups
- Tweak visualizer to client's specification
- Continual testing of all provided assembly programs
- Begin to investigate how to run the provided program to load instructions into the user space from the switches of the altera gui

Aiman -

- Generate new pptx file specifically to showcase Verilog files
- Modify smaller details such as naming conventions within the generated Verilog files
- Add MIT Licenses to the main CPU file for distribution