

Team Name: sdmay21-38

Team Members: Colby McKinley, Aiman Priester, Eric Marcanio, Brady Kolosik, Byrce Snell, Jacob Betsworth

Report Period: Sept 27-March 1st

### Past week accomplishments

- Eric - Assembler
  - Syntax highlighting added for most instructions
  - Table easier to read for a long list of instructions
  - Padding for buttons
  - Assembly numbering for just the code
  - Examples added for multiple programs
  - Below is a view of the assembler when syntax highlighting is on

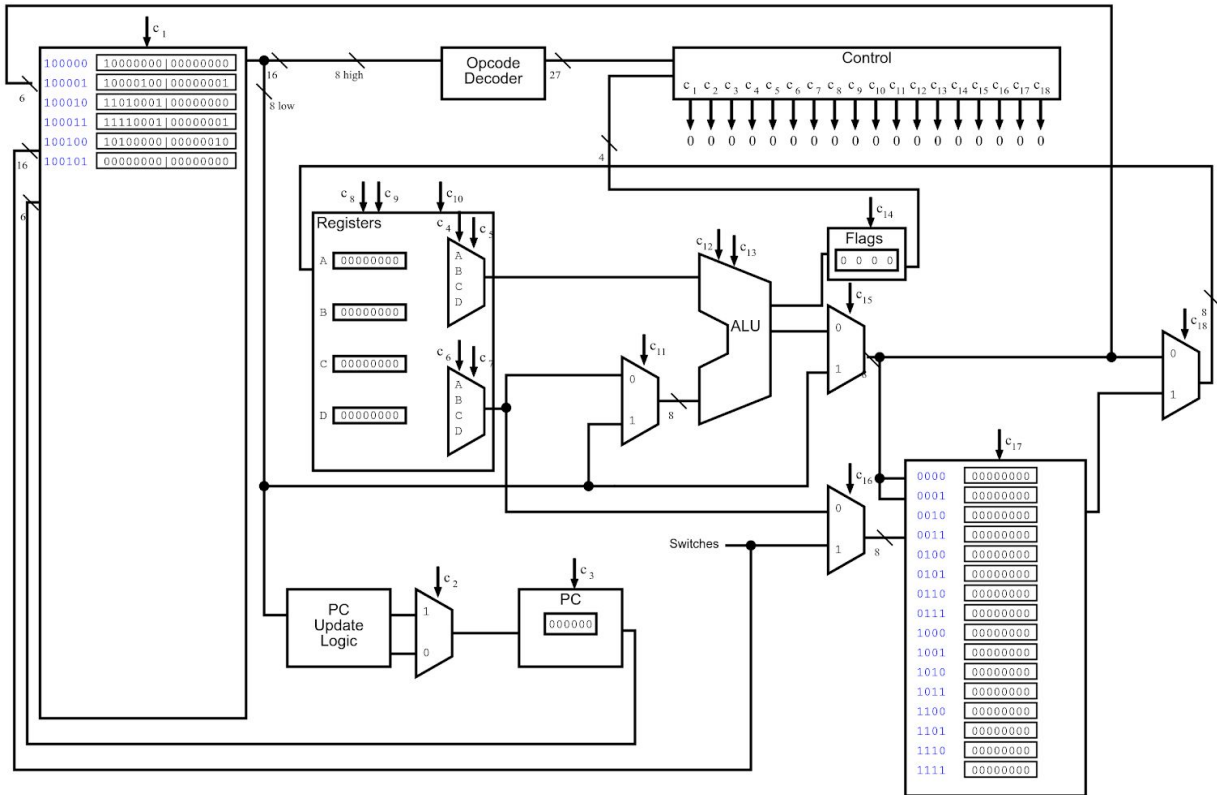
The screenshot shows the i281 Assembler interface. At the top, it says "i281 Assembler" and "Examples". The main heading is "Successfully Assembled". Below this are four buttons: "Download Machine code", "Download Low", "Download High", and "Syntax highlight: ON". The interface is divided into two main sections: "Assembly Code:" and "Machine Code:". The "Assembly Code:" section is further divided into ".data" and ".code". The ".data" section contains a table with columns for label, type, and value. The ".code" section contains a table with columns for instruction number, instruction, operands, and machine code. The "Machine Code:" section is further divided into "Data Memory:" and "Code Segment:". The "Data Memory:" section is currently empty. The "Code Segment:" section contains a table with columns for instruction number, instruction, operands, and machine code.

Assembly Code:			Machine Code:	
.data			Data Memory:	
x	BYTE	5		
min	BYTE	1		
max	BYTE	8		
inRange	BYTE	0		
.code			Code Segment:	
1	LOAD	A [x]	1000_00_00_00000000	
2	LOAD	B [min]	1000_01_00_00000001	
3	LOAD	C [max]	1000_10_00_00000010	
4	CMP	B A	1101_01_00_00000000	
5	BRG	End	1111_00_10_00000100	
6	CMP	A C	1101_00_10_00000000	
7	BRG	End	1111_00_10_00000010	
8	LOADI	D 1	0011_11_00_00000001	
9	STORE	[inRange] D	1010_11_00_00000011	
10	End: NOOP		0000_00_00_00000000	

- Colby - Simulator

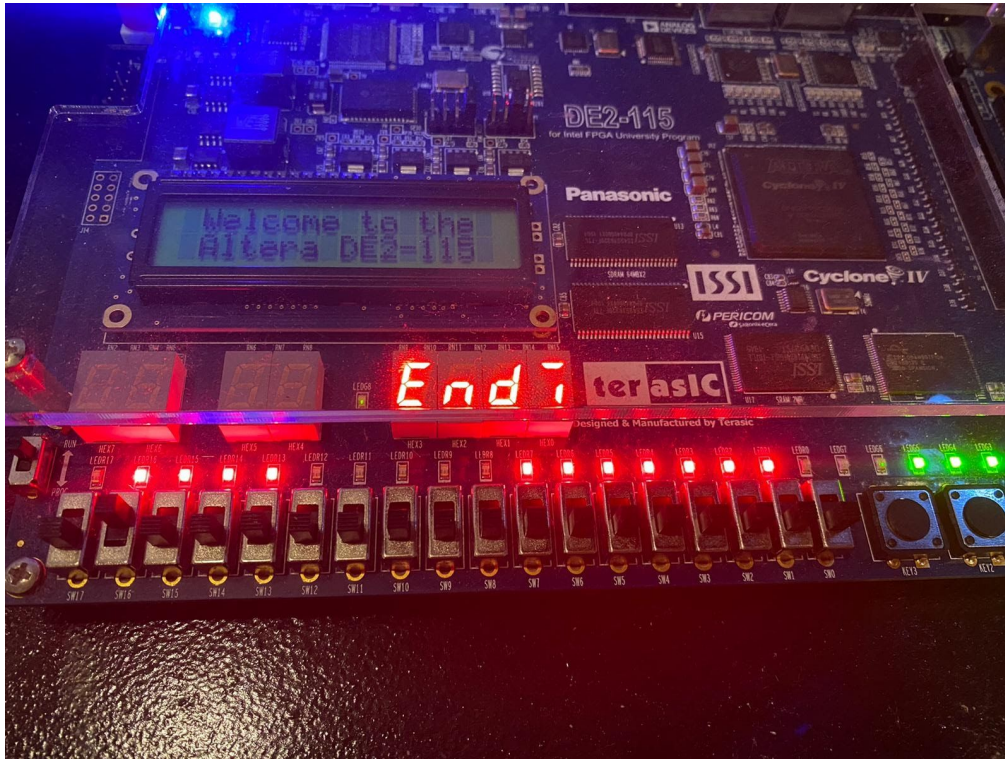
- Continued work on labeling arrows and bus widths. Made slight visual changes to Control. Made ALU 10% bigger.

i281 CPU



- Aiman - Verilog

- Verilog Conversion is complete. The verilog implementation of the i281 processor is able to play a simplified version of pong on the seven segment displays.



- Will work on stress tests with different sorting algorithms in the coming weeks, hoping to find bugs to stomp out.
- Brady - Simulator
  - Added padding for instruction and data memory value boxes, over all rearranged some components and made some space per client request. (see image above from Colby for this example).
  - Continued to implement client requested changes
  - Merged dev branches into master to integrate my features with some of Colby's
  - Segmented wires to allow for easy color changing, this adds junctions and lets the wires be referred to as groups.

```
//IMEM WIRE SEGMENTS
var imem_out_0_wire = new PathSVG("imem_out", Constants.CODE_MEM_OUT_0, Constants.WIRE_STYLE);
var imem_to_decoder = new PathSVG("imem_to_decoder", Constants.TO_OPCODE_DECODER, Constants.WIRE_STYLE);
var imem_to_pc = new PathSVG("imem_to_junction", Constants.PC_MUX_JUNCTION, Constants.WIRE_STYLE);
var to_mux_junction = new PathSVG("to_mux_junction", Constants.MUX_JUNCTION, Constants.WIRE_STYLE);
var to_mux0 = new PathSVG("to_mux_0", Constants.TO_MUX0, Constants.WIRE_STYLE)
var to_update_logic = new PathSVG("to_update_logic", Constants.TO_PC_UPDATE, Constants.WIRE_STYLE)
var to_mux1 = new PathSVG("to_mux_1", Constants.TO_MUX1, Constants.WIRE_STYLE)
//END IMEM WIRE SEGMENTS

//READ A SEGMENTS
var read_a_out = new PathSVG("read_a_out", Constants.READ_A_OUT, Constants.WIRE_STYLE)
//END READ A SEGMENTS

//READ B SEGMENTS
var read_b_out = new PathSVG("read_b_out", Constants.READ_B_OUT, Constants.WIRE_STYLE)
var b_to_mux0 = new PathSVG("b_to_mux0", Constants.B_OUT_TO_MUX0, Constants.WIRE_STYLE)
var b_to_mux2 = new PathSVG("b_to_mux2", Constants.B_OUT_TO_MUX2, Constants.WIRE_STYLE)
//END READ B SEGMENTS

//IMEM MUX2 SEGMENTS
var imem_mux2_junction = new PathSVG("imem_mux2_junction", Constants.IMEM_MUX2_JUNCTION, Constants.WIRE_STYLE)
//END IMEM MUX2 SEGMENTS

//MUX1 SEGMENTS
var mux1_out = new PathSVG("mux1_out", Constants.MUX1_OUT, Constants.WIRE_STYLE)
var mux1_out_to_mux3_imem_junction = new PathSVG("mux1_out_to_mux3", Constants.MUX1_OUT_TO_MUX3_IMEM_JUNCTION, Constants.WIRE_STYLE)
var mux1_out_to_dmем_junction = new PathSVG("mux1_out_to_dmем_junction", Constants.MUX1_OUT_TO_DMЕМ_JUNCTION, Constants.WIRE_STYLE)
var junction_to_dmем_a = new PathSVG("junction_to_dmем_a", Constants.JUNCTION_TO_DMЕМ_A, Constants.WIRE_STYLE)
var junction_to_dmем_b = new PathSVG("junction_to_dmем_b", Constants.JUNCTION_TO_DMЕМ_B, Constants.WIRE_STYLE)
var junction_to_imem = new PathSVG("junction_to_imem", Constants.JUNCTION_TO_IMEM, Constants.WIRE_STYLE)
var junction_to_mux3 = new PathSVG("junction_to_mux3", Constants.JUNCTION_TO_MUX3, Constants.WIRE_STYLE)
//END MUX1 SEGMENTS
```

- Bryce - CPU Simulator
  - Was able to run the first programs through the processor.
  - Tests went far better than expected.

```
Unsorted Array: 00000010, 00000011, 00000100, 00000001
| Sorted Array: 00000100, 00000011, 00000010, 00000001
=====
Total execution time was: 3.1393319964408875 ms
Average time per instruction: 0.02638094114656208 ms
Average "frequency": 37.906153326539616 KHz
```

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- Jacob - Board design
  - Made the new buttons circled in red, made color updates to switch elements, and general code formatting changes



## Pending Issues

Assembler - Eric

- Text needs to be easier to read when syntax highlighting is on
- Data memory needs to be shown when an array is given (Dropdown?)

Aiman

- Clean up and split the files into Verilog and BDF.

## Individual Contributions

<b>Team Member</b>	<b>Contribution</b>	<b>Weekly Hours</b>	<b>Total Hours</b>
<b>Eric Marcanio</b>	Implemented syntax highlighting for the assembler	<b>6</b>	<b>26</b>
<b>Colby McKinley</b>	Started adding display info as described above	<b>8</b>	<b>27</b>
<b>Aiman Priester</b>	Finished verilog conversion	<b>7</b>	<b>27</b>
<b>Brady Kolosik</b>	Wires segmented, various visual changes to the display following client requests.	<b>8</b>	<b>20.5</b>
<b>Bryce Snell</b>	Demonstrated functionality of CPU simulator	<b>7</b>	<b>25</b>
<b>Jacob Betsworth</b>	Made more buttons and formatted code	<b>6</b>	<b>17</b>

### **Plans for Upcoming Reporting Period**

Eric - Implement syntax highlighting for the store key word and fix formatting for the data memory

Jacob- Add triangles to edges of segment lines and make it possible to press multiple buttons at once

Aiman - Continue testing edge cases to stomp out bugs within the implementation.

Bryce - Begin integrating with rest of the team

Colby - Finish added bus width info to all wires. Move around components according to client. Start work on the arrows update.

Brady- Center certain wires about multiplexers, fix flags wires to be centered, Increase register box size, have selector line within multiplexers. Move wires to accommodate bus lengths that Colby is developing. Begin the process of integration between simulator, assembler, and visualizer. Run experiments to change values in text fields to avoid reassembling code for small changes.

